ASYNCHRONOUS ANALOG-DISCRETE CONVERTER USING AN ANALOG SIGNAL PROCESSOR STABILIZED IN AN INFLECTION POINT

Sabiniano Araujo Rodrigues [1], *José Ivan Carnaúba Accioly* [2]*, Raimundo Carlos Silvério Freire* [3]*, Isaac Maia Pessoa* [4]

[1] CEFET-PB, João Pessoa-PB, Brazil, saraujo.pb@uol.com.br
[2] CEFET-PB, João Pessoa-PB, Brazil, josehaccioly@gmail.com
[3] UFCG, Campina Grande-PB, Brazil, rcsfreire@de.ufcg.edu.br
[4] UFCG, Campina Grande-PB, Brazil, isaac@dsc.ufcg.edu.br

Abstract: This brief article presents the architecture and the implementation of a converter of analog signals into discrete signals of three levels, asynchronous, with sample frequency in the gigahertz band. To make possible the implementation of this converter, it was projected and also implemented an analog signals processor that functions stabilized round an inflection point, in substitution to the operational amplifiers used in the first version of the converter and that allowed to work with high gain and slew-rate. This processor is also described in this article.

Keywords: converter, asynchronous, gigahertz. (maximum of three).

1. INTRODUCTION

The connection of digital circuits to the sensors is simple if the sensors are inherently digital. Keys, relays and decoders are easily interfaced with digital circuits due to the on-off nature of its signals. However, when the analog components are involved, the interface becomes much more complex, being then necessary a way of transforming eletronically the signals from the analog form for the digital one. For this the analog-digital converters (CAD) and the digital-analog converters (DAC) are used. All these architectures possess their advantages and their disadvantages serving better to some applications than others.

The folding A/D converters and interpolation of signals had revealed efficient means for digitalization of signals of raised width of band and intermediate resolution, as presented in [1]. In comparison with architectures (flash) entirely parallel, they require few comparators while they keep the advantages of high speed and low latency. Due to the reduced number of the required comparators, converters of architectures that use the folding and the interpolation are good candidates for implementations of A/D converters of low power, average resolution (6 to 10 bits) and high speed (tens to hundreds of mega-sample/s). The reduction in the number of comparators is gotten by the use of folding amplifiers, while the interpolation is used to keep the number of such amplifiers small. Although such converters have been initially developed using bipolar technology [2] - [7], a great number of implementations using metal-oxide complementary semiconductor (CMOS) [8] - [16] and BiCMOS [13], [14] are reported.

2. CONVERTER

The proposed converter makes a folding of the input analog signal. Being inserted in the first block of A/D converter, the input analog signal is "packed" or "folded", with its adjusted limit tensions into Vref+ e Vref-. This folding occurs while making a comparison between the input analog signal and values of tension of reference adjusted in the first block of A/D converter proposed through the Vref+ e Vref- inputs.

This process of folding occurs in each block. And each block represents an output from discrete signal. That is, if a converter with ten discrete outputs is implemented, it will have ten blocks of signal folding and this same input analog signal will be presented in the output of the tenth block folded ten times.

If we consider that f(t) is a continuous function in time, that describes the input analog signal of the first block, after the function f(t) pass in the folding circuit, we will have in the output of the first block a function that can be called folded function of f(t) around a Kj constant. If to this folded function of f(t) the name of O(t) is given, we have, associated to this function O(t), a discrete signal of three levels called D(t).

The flowchart presented in the figure 1 shows each step of the conversion process of the analog signal (f(t)) into a discrete signal (D(t)) and other analog signal (O(t)).
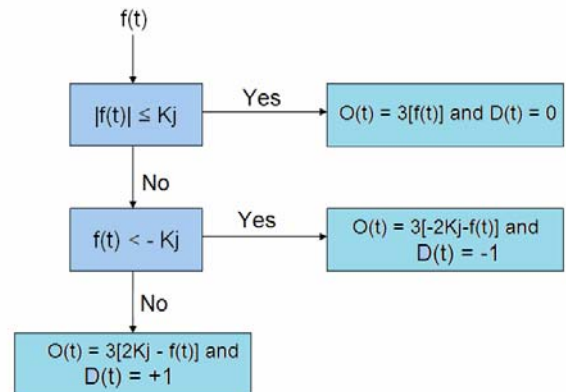

Fig. 1 – Flowchart of the conversion process.

D (t) and O(t) are defined in way that

$$O(t) = 3\,f(t)\ e\ D(t) = 0 \qquad (1)$$

when module of f(t) will be lesser or equal to Kj,

$$O(t) = 3\,[2Kj - f(t)]\ e\ D(t) = 1 \qquad (2)$$

when f(t) > Kj, and

$$O(t) = 3\,[-2Kj - f(t)]\ e\ D(t) = -1 \qquad (3)$$

when $f(t) < - Kj$.

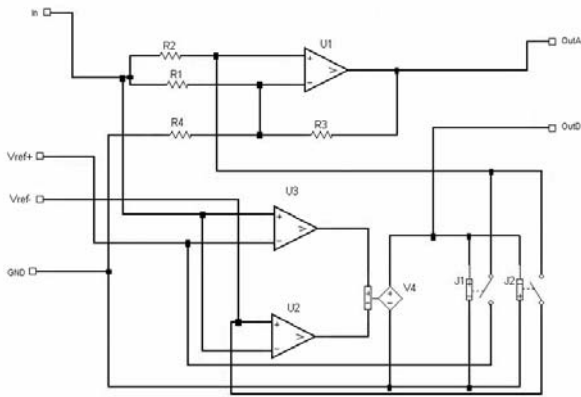The figure 2, as follows, shows the circuit of initial implementation of the first block of the considered converter.

Fig. 2 – circuit of the first block of the proposed converter.

In this configuration a relation must be kept of R, nR and nR/n-1 among the three resistors R1, R3 and R4, respectively. Keeping this relation, we will have a gain of closed mesh varying between –n and +n. R1 and R2 have the same value. In this converter, the value of n was adjusted in 3.

The configuration will vary in three different ways, depending on the value of the input signal. In the first case, where the value of the input signal is among Vref+ and Vref– (Vref– < f(t) < Vref+), the amplifier is in an operational configuration shown in Figure 3 below.

In this case we have the keys J1 and J2, in the circuit of Figure 2, open, because the voltage that the comparator place at the source of tension controlled by tension (V4) is not enough to close the keys. Then we have the Ot) = 3f(t).
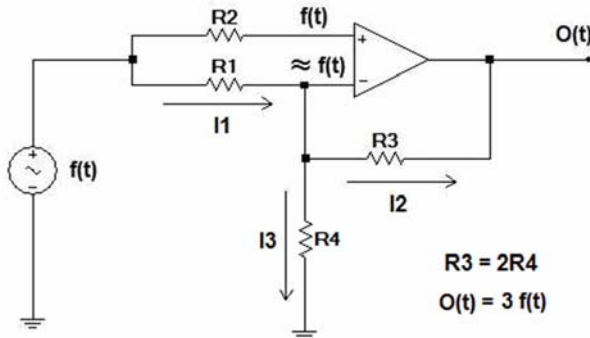

Fig. 3 – Configuration of the circuit of the first block of the considered converter, in the first form of the configuration.

In the second case, where the input signal is bigger then positive reference value (Vref+), the operational amplifier(op-amp) is configured as shown in the figure 4 as following.

In this case the switch J1 is closed and the switch J2 is opened(circuit of figure 2). It results in the voltage Vref+ in the positive terminal of the operational amplifier. Therefore we have O(t) = 3 [2 (Vref+) – f(t)]. The Kj is the module value of the reference voltage (Vref), so we have O(t) = 3[2Kj – f(t)].
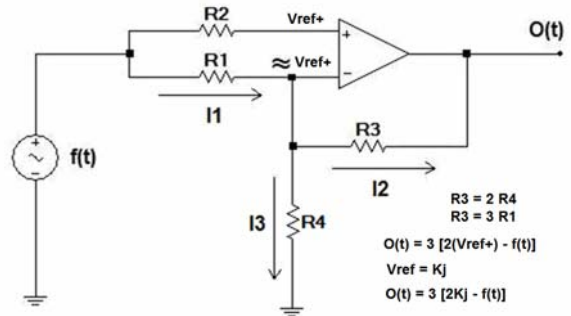

Fig. 4 – Configuration of the circuit of the first block of the considered converter, in the second form of the configuration.

In the third case, where the input signal is smaller then negative reference value (Vref-), the operational amplifier is configured as shown in the figure 5 as following.

In this case, the switch J1 is opened and J2 is closed(circuit of figure 2). It results in the voltage Vref- in the positive terminal of the operational amplifier. Therefore we have O(t) = 3 [2 (Vref–) – f(t)]. The Kj is the module value of the reference voltage (Vref), so we have O(t) = 3[–2Kj – f(t)].
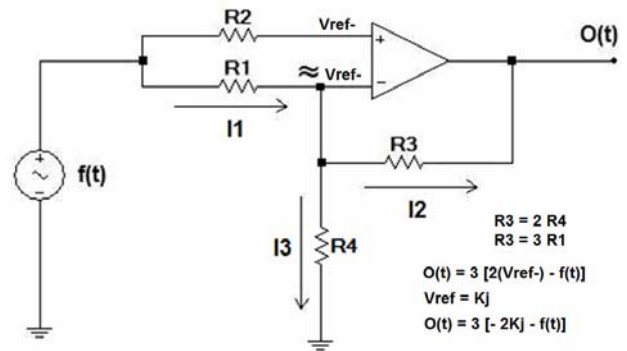

Fig. 5 – Configuration of the circuit of the first block of the considered converter, in the third form of the configuration.

In figure 6 as follows, the forms of wave of the input signal and the analog and discrete outputs of the first block are shown.
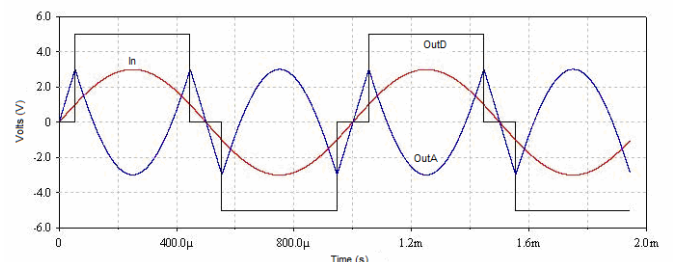

Fig. 6 – Forms of input wave and of the analog and discrete exits.

From the fourth block of the converter, a distortion presented in the output analog signal is noticed. This distortion is due to the fact of the slew rate of the operational amplifier not follow the variation of the input signal. The parameters chosen for the operational amplifier and for the comparators had been similar to the parameters of LF357, that is an operational amplifier with JFET input. According to the list of data of this operational, its slew rate is of the order of 50V/μs. This operational amplifier is considered of fast reply and therefore it was used in our simulations.

In figure 7 as follows, the form of wave of the analog signal of the fourth block is shown.
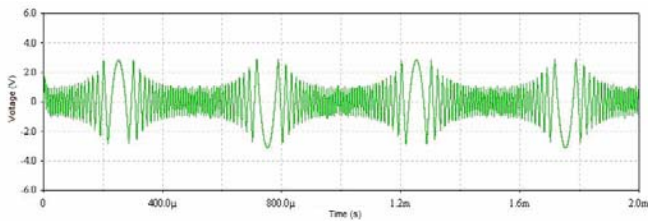

Fig. 7 – Forms of the analog signal wave of the fourth block

It was necessary, then, the development of a processor of signals that functioned in similar way to an operational amplifier and that it had its characteristics extremely improved, mainly the gain of open mesh and slew rate.

3. ANALOG PROCESSOR OF SIGNALS

The model of the proposed analog processor is based on the operation of an amplifier around an inflection point. To this amplifier the transinflexor name was given. In figure 8 a possible model of implementation of an amplifier is shown with this characteristic.
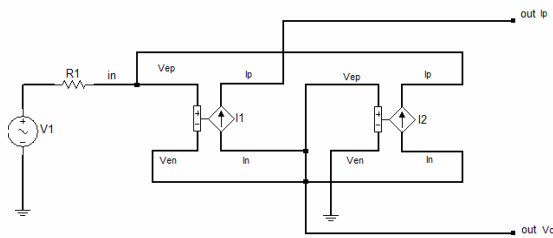

Fig. 8 – Model of the implementation of transinflexor.

The transinflexor is composed of two current sources controlled by voltage, with some terminals connected into a positive feedback and a total negative feedback in order to create the virtual ground in the input, compensating all variation of the analog input signal.

The second current source works like a charge for the first source.

For the explanation of the open loop gain, we placed two resistors in the transinflexor, the first one for feedback and the other for charge, we placed too the output voltage Vc connected directly to the ground as shown in the figure 9.
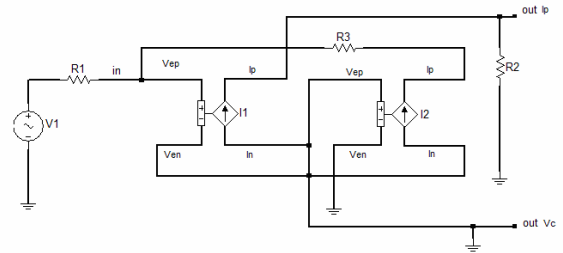

Fig. 9 – Model of implementation of the transinflexor with the feedback and charge resistors.

The gain of open mesh of the model shown in figure 4 is given by:

$$OLG = \frac{V_s}{V_1} = -\frac{G_{m1} \cdot G_{m2} \cdot R3 // R_2}{1 - G_{m2}} \qquad (4)$$

where Gm_1 is the transconductance of the first current source controlled by a differential voltage source, Gm_2 is the transconductance of the second current source controlled by a differential voltage, R2 is the charge resistor and R3 is the feedback resistor. In the model there is still the R1 resistor that is the input of the model, but R1 wasn't shown in the expression; it is used only for limit the input current coming of the source V1. The values of R1, R2 and R3 can be 1 KΩ.

The inflection point, where the gain will be infinite, happens when $Gm_2 = 1$. It is next to this point that the considered processor will work.

In figure 10 as follows, it is shown a transinflexor implemented with four bipolar transistors that function next to the inflection point.
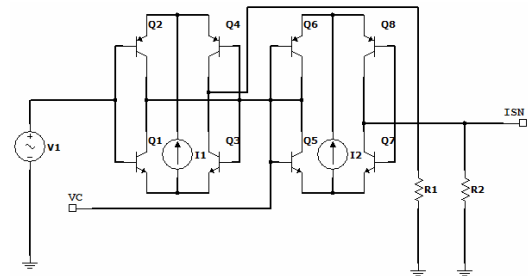

Fig. 10 – Model of implementation of transinflexor.

In figure 11 the wave forms of simulation are shown. The forms of wave of the input signal and of the output signals and a signal of control that will be necessary later for the purpose of limitations of tensions and of currents for the use in the converter .
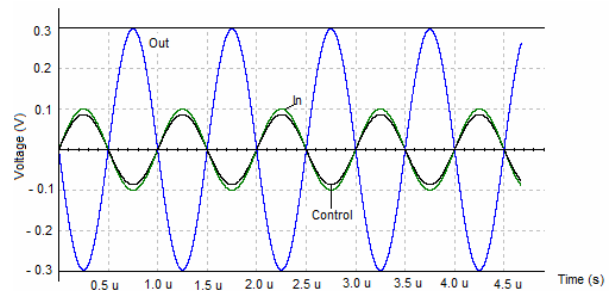

Fig. 11 – Forms of wave from the transinflexor.

In the circuit of figure 9 the values of R1 and R2 are 100 Ω and 300 Ω, respectively. Since that the transinflexor works according to the forms of wave of figure 11, the model can be examined through diagrams of flows. In figure 12 as follows, the diagram of flows of the model of the transinflexor presented in the figure 9 is shown.
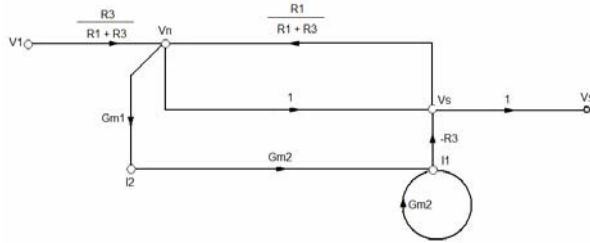
Fig. 12 – Diagram of flows of the figure 4 model.

The relation between V_S and I_2 shown in diagrams of flows is:

$$\frac{V_S}{I_2} = \frac{-R_3 \cdot G_{m2}}{1 - G_{m2}} \tag{5}$$

The determinant of the two closed meshes is:

$$\Delta = \frac{1}{1 - b + \dfrac{G_{m1} \cdot R3 \cdot G_{m2} \cdot b}{1 - G_{m2}}} \tag{6}$$

With this result, the equation for the gain signal is:

$$\frac{V_S}{V_1} = \frac{a - \dfrac{R3 \cdot G_{m2} \cdot G_{m1} \cdot a}{1 - G_{m2}}}{1 - b + \dfrac{G_{m1} \cdot R3 \cdot G_{m2} \cdot b}{1 - G_{m2}}} \tag{7}$$

In which

$$a = \frac{R3}{R1 + R3} \tag{8}$$

and $b = \dfrac{R1}{R1 + R3}$ (9)

Calculating the limit of X tending to 1, that it is the inflection point, we have

$$\lim_{G_{m2} \to 1} \frac{V_S}{V_1} = \frac{-a}{b} = -\frac{R3(R1 + R3)}{(R1 + R3)R1} = -\frac{R3}{R1} \tag{10}$$

This shows that the gain will always be steady next to the inflection point. If $G_{m2} > 1$, the gain will be positive. If $G_{m2} < 1$, the gain will be negative. And if $G_{m2} = 1$, the gain will be infinite, that defines the inflection point. In all the simulations the gain always varied close to the inflection point. In some moments being positive and in others being negative. This analog processor made possible the implementation of the converter of analog signals in discrete signals of three levels. Therefore the high gain and excellent slew rate had given the propitious conditions for the functioning of the converter.

4. CONVERTER WITH TRANSINFLEXOR

In figure 13 as follows it is shown the whole circuit using the transinflexor. All processing of this converter was done by current. The processing is the same shown in the item 2, where it is explained by the voltage signals.
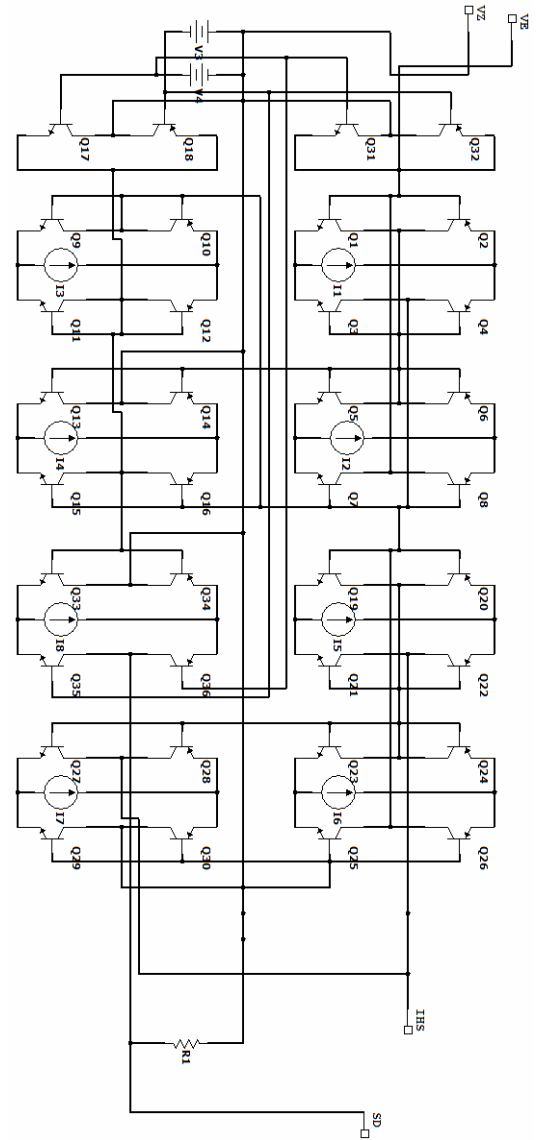
Fig. 13 – Model of implementation of converter using the transinflexor.

This circuit has two inputs and two outputs. An input for the analog signal (VE) and an input for the reference signal (ground) (VZ). And an output analog, where the folded hybrid signal (IHS) leaves, and an output for the digital signal (SD). The signal ISH is a current signal.

This circuit can be divided into blocks with the specific functions for each one, but is important to take care that there isn't separated functionalities, because of the dependence of each one.

The block with transistors Q1 to Q8 results the first transinflexor and Q19 to Q26 results in the second transinflexor. The current source I1 to I5 have the value 4mA and the current sources I2 and I6 have the value 3.85 mA. This difference occur in the consumed current in the polarization of the bipolar transistors. This values were chosen for a variation of the input current signal between +3mA and -3mA. The blocks of the current sources I4 and I7, the transistors Q13 to Q16 and Q27 to Q30, respectively, are two multipliers by two. They works by multiplying the currents of transinflexors. The current sources values I4 and

I7 are 8mA. The multiplier of the current source I7, is working as a half multiplier. The result is a multiplication by three of the current of input signal as shown in the flowchart of the figure 1.

The block with current source I3 and the transistors Q9 to Q12, works as current limit. If the current will be bigger of 2 mA, the value of the current adjusted in source I3, the current signal will appear in the exit. If it will be lesser, the current will pass all for this block directly going to the ground. This block has the function to take boundary-values to the inputs of transinflexors. It makes the control of the inversion of the current in transinflexors when it arrives at third part of the value of the maximum output current. As the maximum output current varies between + 6 mA and – 6 mA, after multiplied for two, the inversion is made when it reaches 2 mA.

The block formed for the current source I8 and transistors Q33 to Q36, is the responsible block for the generation of the discrete output signals. As the value of the current source I8 is 1 mA, this will be the output current of the discrete signals. In the case of the circuit of the figure 13 as follows, the value of the resistor R1 is 200 Ω. Then the discrete output signal varies between +200 mV and – 200 mV.

The blocks formed for the transistors Q17 and Q18, and Q31 and Q32 have the function to prevent that the transistors reach the saturation tension. For this, they are fed with sources of reference of + 300 mV and – 300 mV, in this specific case. When the tension of collector of the transistors exceeds this value, this block generates a current in contrary direction, diminishing the collector tension, thus preventing the saturation of the transistors.

Each block of the converter contains an identical circuit to this, that makes all the processing in an analog form and with the output of the discrete signal occurring in an independent form of the analog processing. And this circuit follows the algorithm defined in the flowchart of the figure 1. In figure 14 as follows the forms of output wave of the tenth block of the converter are shown.
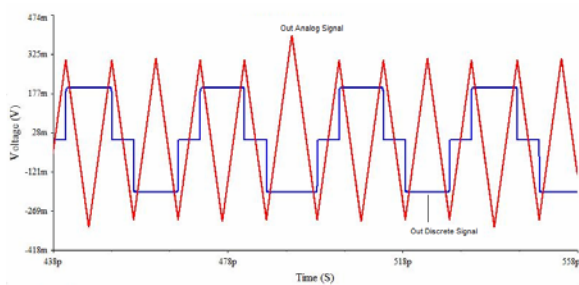
Fig. 14 – Output of the tenth block of the converter

5. RESULTS

Comparisons and measurements of some values presented in the majority of the analog-digital converters produced currently had been made, such as sampling frequency and resolution and of two common parameters of operational amplifiers as gain and slew-rate.

Converters	Sample frequency	Resolution
With aoperational amplifiers	~ 100 MHz	Up to 5 bits
With Transinflexor	~ 10 GHz	> 10 bits

Table 1. Parameters of converters.

Amplificadores	Gain	Slew-rate
Operacional Amplifier (HA-2539)	15 KV/V	600 V/µs
Transinflexor	~ 100 KV/V	8 KV/µs

Table 2. Parameters of processors.

After carried through the measures of tables 1 and 2, measurements in the complete circuit of the converter had been made, with ten discrete outputs. Figure 15, as follows, shows the diagram of blocks of the complete converter.
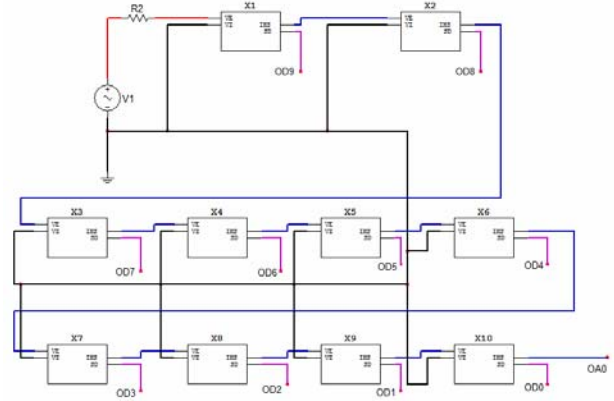
Fig. 15 – Diagram of blocks of the complete converter

The Fourier analysis of the presented hybrid output signal of the last block was measured, because it is the signal that presents values of tension in the greats component of frequency of the circuit. Figure 16, as follows, shows the graph of this measure, where we can take off the data contained in table 3, also as follows.
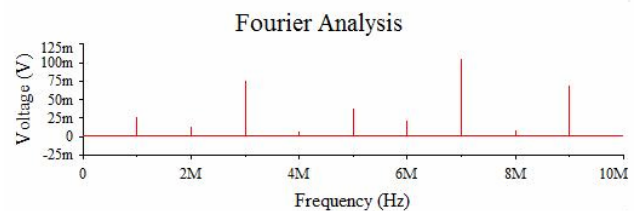
Fig. 16 – Fourier analysis of the hybrid output signal of the last block.

Harmonic	Frrequency (Hz)	Magnitude (V)	Phase (º)
1	1e+006	0.0251414	7.75909
2	2 e+006	0.0126339	21.5896
3	3 e+006	0.0753474	171.139
4	4 e+006	0.00555319	146.763
5	5 e+006	0.0368014	-2.168
6	6 e+006	0.0210082	159.334
7	7 e+006	0.103305	-175.21
8	8 e+006	0.0073417	-74.442
9	9 e+006	0.068633	-4.3513

Table. 3 – Values of the Fourier analysis of the hybrid output signal of the last block.

The measures made in the analog-discrete converter of ten outputs, are summarized in table 4, as follows.

Vdd	3,3 V
Resolution	10 ternary bits
Conversion rate	11.7 GS/s
Input range	± 300 mV
Power dissipation	80 mW

Table. 4 – Parameters applied and measured in the converter

The values of the measurements in the converters and amplifiers had been obtained through simulations carried through the software of simulation of electronic circuits NI Electronics Workbench Group 10.0.1 Version Academic Software.

6. CONCLUSION

This project is part of the PhD thesis of the first author of this article, and the simulation part was finished. Currently it is in the phase of transference of the circuit, in blocks for CMOS technology aiming at a possible manufacture of an integrated circuit.

A great difficulty in the beginning of the work existed, therefore, similar reference to the initial idea of the project was not found. From the beginning of the activities, some articles were found approximately in this area of development.

The values measured in the simulations had been excellent and with great advances in terms of processing speed in relation to the products found in the market.

REFERENCES

[1] Sotirios Limotyrakis, KiYoung Nam, and Bruce A. Wooley, "Analysis and Simulation of Distortion in Folding and Interpolating A/D Converters", IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 49, nº. 3, março 2002.

[2] R. E. J. van de Grift and R. J. van de Plassche, "A monolithic 8-bit video A/D converter," IEEE J. Solid-State Circuits, vol. SC-19, pp. 374–378, June 1984.

[3] R. E. J. van de Grift, I. W. J. M. Rutten, and M. van der Veen, "An 8-bit video ADC incorporating folding and interpolation techniques," IEEE J. Solid-State Circuits, vol. SC-22, pp. 944–953, Dec. 1987.

[4] R. J. van de Plassche and P. Baltus, "An 8-bit 100-MHz full-Nyquist analog-to-digital converter," IEEE J. Solid-State Circuits, vol. 23, pp. 1334–1344, Dec. 1988.

[5] J. van Valburg and R. J. van de Plassche, "An 8-b 650-MHz folding ADC," IEEE J. Solid-State Circuits, vol. 27, pp. 1662–1666, Dec. 1992.

[6] W. T. Colleran and A. A. Abidi, "A 10-b, 75-MHz two-stage pipelined bipolar A/D converter," IEEE J. Solid-State Circuits, vol. 28, pp. 1187–1199, Dec. 1993.

[7] W. An and C. A. T. Salama, "An 8-bit, 1-Gsample/s folding-interpolating analog-to-digital converter," in Proc. 26th European Solid-State Circuits Conf., Sep. 2000, pp. 200–203.

[8] B. Nauta and A. G.W. Venes, "A 70-MS/s 100-mW 8-b CMOS folding and interpolating A/D converter," IEEE J. Solid-State Circuits, vol. 30, pp. 1302–1308, Dec. 1995.

[9] R. Roovers and M. S. J. Steyaert, "A 175 Ms/s, 6 b, 160 mW, 3.3 V CMOS A/D converter," IEEE J. Solid-State Circuits, vol. 31, pp. 938–944, July 1996.

[10] M. P. Flynn and D. J. Allstot, "CMOS folding A/D converters with current-mode interpolation," IEEE J. Solid-State Circuits, vol. 31, pp. 1248–1257, Sept. 1996.

[11] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing," IEEE J. Solid-State Circuits, vol. 31, pp. 1846–1853, Dec. 1996.

[12] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1 mm ," IEEE J. Solid-State Circuits, vol. 32, pp. 1887–1895, Dec. 1997.

[13] M. Flynn and B. Sheahan, "A 400-Msample/s, 6b CMOS folding and interpolating ADC," IEEE J. Solid-State Circuits, pp. 1932–1938, Dec. 1998.

[14] M. J. Choe, B. S. Song, and K. Bacrania, "An 8-b 100-MSample/s CMOS pipelined folding ADC," IEEE J. Solid-State Circuits, vol. 36, pp. 184–194, Feb. 2001.

[15] Andrew M. Abo and Paul R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", IEEE J. Solid-State Circuits, vol. 34, no. 5, May 1999.

[16] Luca Picolli, Andrea Rossini, Piero Malcovati, Franco Maloberti, Fausto Borghetti and Andrea Baschirotto, "A Clock-Less 10-bit Pipeline-Like A/D Converter for Self-Triggered Sensors", IEEE J. Solid-State Circuits, vol. 43, no. 2, February 2008.