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SIGNATURE ANALYSIS FOR MEMS PSEUDORANDOM TESTING USING NEURAL NETWORKS

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Abstract: The aim of this work is to develop a low-overhead, low-cost built-in test for Micro Electro Mechanical Systems (MEMS). The proposed method relies on processing the Impulse Response (IR) through trained neural networks, in order to predict a set of MEMS performances, which are otherwise very expensive to measure using the conventional test approach. The use of neural networks allows us to employ a low-dimensional IR signature, which results in a compact built-in test. A MEMS structure combining electro-thermal excitation and piezoresistive sensing was chosen as our case study. A behavioral model of this structure was built using Matlab for the purpose of the experiment. The results demonstrate that the neural network predictions are in excellent agreement with the simulation results of the behavioral model.

Keywords: MEMS testing, neural networks, feature selection.

1. INTRODUCTION

MEMS are used as building blocks in various sensors and actuators. These blocks are made by micromachining and contain mechanical elements and converters which operate in multiple energy domains, such as mechanical, thermal and electrical [1]. As an example, the cantilever structure, shown in Figure 1, combines electro-thermal actuation and piezoresistive sensing.

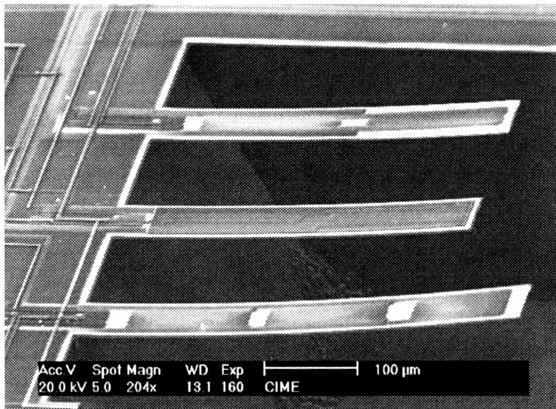

Fig. 1: MEMS structure [2]

The production test of devices employing MEMS structures is based on direct measurement of performance parameters such that the specifications promised in the data sheet are met. Such measurement procedures require the use of sophisticated and expensive external test equipment. For example, mechanical vibrations need to be applied.

An alternative approach to obtain specification parameters based on IR evaluation was developed in [3]. The aim is to substitute the expensive thermal and mechanical tests with a simple pseudorandom test, as shown in Figure 2. Specifically, the MEMS device is embedded between an ADC and a DAC. The DAC is driven by a pseudorandom sequence x[k] that is generated by a maximal-length shift register. It can be shown that the cross-correlation between x[k] and the output of the ADC, y[k], is proportional to the IR sample h[k]. The resources required for the on-chip IR evaluation are proportional to the number of estimated samples h[k]. In order to decide on the satisfaction or violation of the specifications, the IR signature is compared to thresholds imposed around a golden signature (i.e. a signature that ideally would include the whole population of functional devices). Clearly, this may result in misclassification since the true boundaries are likely to be very complex.

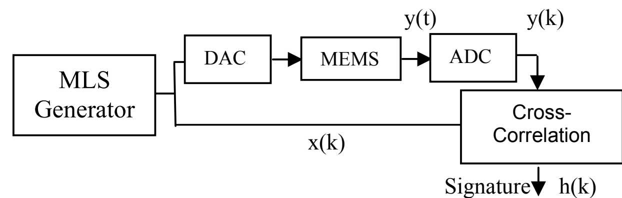

Fig. 2: Pseudorandom test architecture

In this work, we examine the possibility of mapping a reduced number of samples h[k] implicitly to the performance parameters. This mapping is learned by training a feed-forward neural network, as shown in Figure 3. After training is complete, the network is pruned, without deteriorating the mapping resolution, in order to minimize the number of required samples h[k], thereby minimizing the number of correlation cells in the cross-correlation block. This results in a compact built-in test implementation.

We should note that the mapping method follows the alternate test paradigm proposed in [4].

2. METHOD

The electrical equivalent scheme of the cantilever structure of Figure 1 is shown in Figure 4. This parametrized behavioral model can be used for simulating the MEMS structure. Our method consists of the following steps:

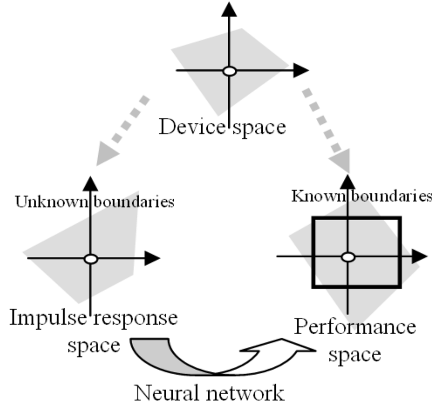

Fig. 3: Mapping IR to the performance space

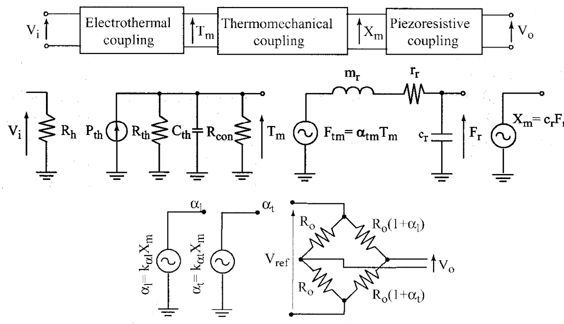

Fig. 4: MEMS electrically equivalent scheme [3]

1) We generate a large number of MEMS instances by carrying out a Monte Carlo simulation of the behavioral model.

2) We determine a training set comprising the IR signature (k=0,.., 40) and the performance parameters for each of these randomly generated instances. We considered the DC gain, the mechanical resonance frequency of the cantilever, *f_mech*, and the low-limiting frequency, *f_therm*, beyond which the cantilever displacement roll-off is observed due to the thermal effect. Generated IRs for 1000 instances are illustrated in Figure 5.

3) We construct a neural network to map the impulse response signature to the performance parameters. We experimented with multi-layer perceptron networks (MLPN) with one and two hidden layers of units, that is, with three and four layers of adaptive weights, respectively.

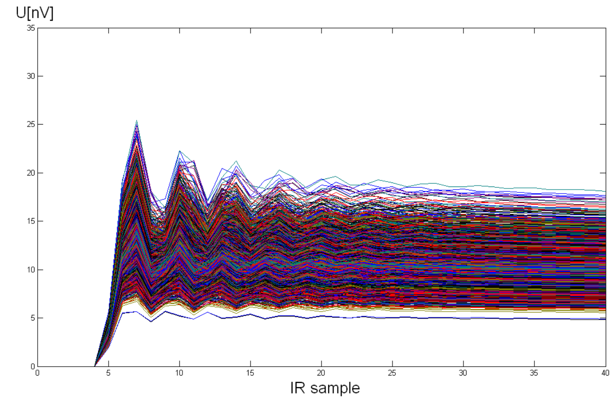

Fig. 5: IRs from MEMS behavioral model simulation

3. RESULTS

The MLPNs are constructed using Matlab v.7.0. The first step is to find the optimal architecture of the 3-layer and 4-layer MLPNs. In particular, the Mean Squared Error (MSE) on an independent testing set initially decreases as we keep adding neurons and at some point it starts increasing, implying that the MLPN becomes too flexible and starts fitting too much of the noise on the training set. This is shown in Figure 6 for the 3-layer MLPN and in Figures 7-8 for the 4-layer MLPN. From these plots it can be deduced that the optimal architectures for the MLPNs in terms of minimum MSE are 40-5-3 and 40-5-5-3.

The next step is feature selection to prune all redundant input neurons and, thereby, eliminate redundant samples h[k]. This is useful since it might improve generalization by mitigating the curse of dimensionality and, in addition, it will allow us to have a simpler structure for possible on-chip realization of the cross-correlation block. A well-known method for this purpose is the contribution measure described in [5].

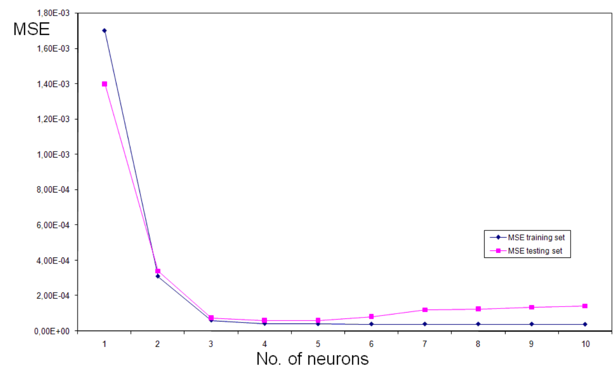

Fig. 6: MSE function of 3-layer MLPN during search of optimal architecture

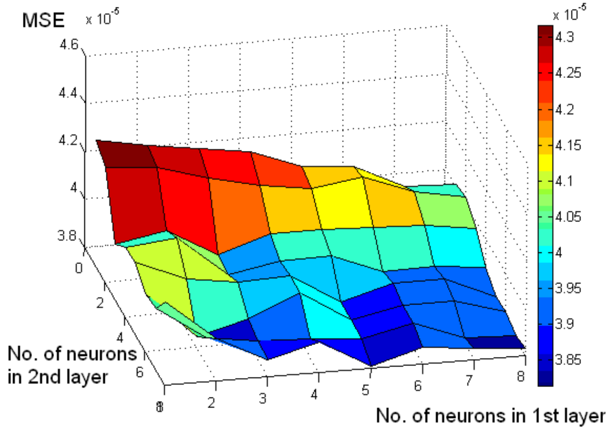

Fig. 7: MSE function of 4-layer MLPN during search of optimal architecture – *Training set*

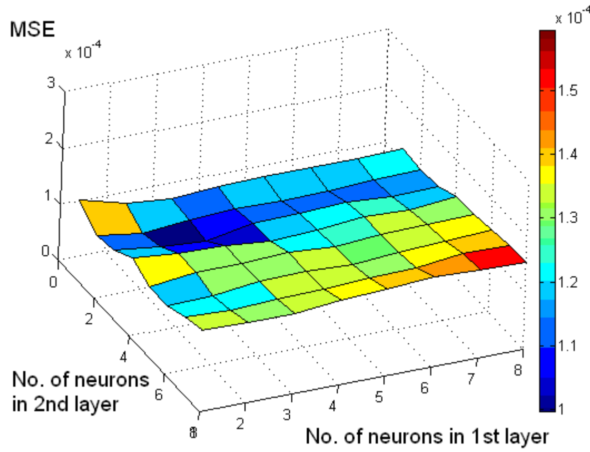

Fig. 8: MSE function of 4-layer MLPN during search of optimal architecture – *Testing set*

For a 3-layer MLPN, the contribution measure of an input node i to an output node k is defined as follows:

$$C_{ik} = \frac{\sum_{j=1}^{N_{hid}} \frac{w_{ij}}{\sum_{l=1}^{N_{in}} \left| w_{ij} \right|} w_{jk}}{\sum_{m=1}^{N_{in}} \left(\sum_{j=1}^{N_{hid}} \left| \frac{w_{mj}}{\sum_{l=1}^{N_{in}} \left| w_{ij} \right|} w_{jk} \right| \right)}, \quad (1)$$

where N_{in} is the number of nodes in the input layer, N_{hid} is the number of nodes in the hidden layer, W_{ij} is the weight on the synapse between an input node i and a hidden node j and W_{jk} is the weight on the connection between a hidden node j and an output node k. The generalization of eq. (1) for the case of a 4-layer MLPN is straightforward.

The contribution measure of an ith input node to the N_{out} output nodes can be calculated as follows:

$$C_i = \sum_{k=1}^{N_{out}} \left| C_{ik} \right|. \quad (2)$$

In each step of pruning it is necessary to calculate the C_i index, in order to find the input neuron with the lowest contribution. This neuron is eliminated and the network is retrained to recalculate the MSE. The procedure terminates when the MSE begins to grow. The first step of this procedure is illustrated in Table 1 for 3-layer MLPN and in Table 2 for 4-layer MLPN, respectively. The course of pruning and the moment where the MSE starts growing are illustrated in Figure 9 for 3-layer MLPN and in Figure 10 for 4-layer MLPN, respectively.

No. of node	C_i	sorted data: No. of node	sorted data: C_i
1	0	1	0
2	0	2	0
3	0	3	0
4	0	4	0
5	0,2264	24	0,04768
6	0,05065	17	0,04836
7	0,06996	6	0,05065
8	0,09659	29	0,05278
9	0,08088	14	0,05341
10	0,11566	36	0,05512
11	0,12139	20	0,05681
12	0,10192	32	0,05781
13	0,08324	33	0,06031
14	0,05341	34	0,06047
15	0,16131	30	0,06142
16	0,0826	28	0,06204
17	0,04836	31	0,06458
18	0,08097	27	0,06824
19	0,08081	7	0,06996
20	0,05681	40	0,0702
21	0,08198	22	0,076
22	0,076	38	0,07675
23	0,08304	19	0,08081
24	0,04768	9	0,08088
25	0,08284	18	0,08097
26	0,11892	21	0,08198
27	0,06824	16	0,0826
28	0,06204	25	0,08284
29	0,05278	23	0,08304
30	0,06142	13	0,08324
31	0,06458	39	0,09605
32	0,05781	8	0,09659
33	0,06031	12	0,10192
34	0,06047	37	0,10214
35	0,11069	35	0,11069
36	0,05512	10	0,11566
37	0,10214	26	0,11892
38	0,07675	11	0,12139
39	0,09605	15	0,16131
40	0,0702	5	0,2264

Table 1: First step of C_i index calculation for the 3-layer MLPN

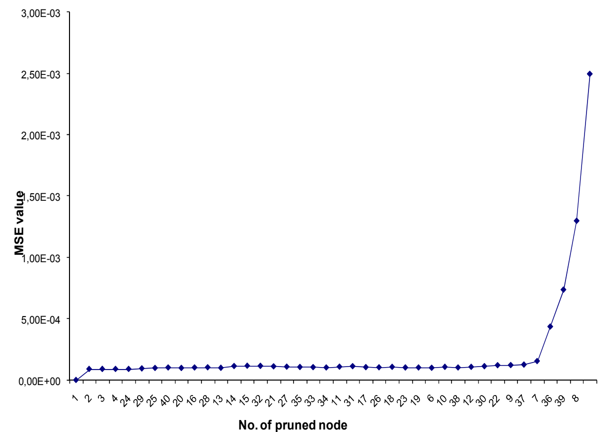

Fig. 9: MSE for the 3-layer MLPN during pruning

No. of node	C_i		sorted data No. of node	sorted data C_i
1	0		1	0
2	0		2	0
3	0		3	0
4	0		4	0
5	0,15342		21	0,0144
6	0,04828		17	0,01793
7	0,03654		20	0,01795
8	0,06189		22	0,02931
9	0,08518		33	0,03008
10	0,0449		35	0,03196
11	0,06919		27	0,03448
12	0,07233		31	0,03484
13	0,04287		7	0,03654
14	0,05758		36	0,03774
15	0,06359		16	0,03993
16	0,03993		24	0,03999
17	0,01793		38	0,04163
18	0,04836		29	0,04182
19	0,0453		13	0,04287
20	0,01795		26	0,04346
21	0,0144		10	0,0449
22	0,02931		19	0,0453
23	0,05162		30	0,04613
24	0,03999		6	0,04828
25	0,04857		18	0,04836
26	0,04346		25	0,04857
27	0,03448		23	0,05162
28	0,05905		14	0,05758
29	0,04182		28	0,05905
30	0,04613		39	0,05953
31	0,03484		8	0,06189
32	0,06968		34	0,06305
33	0,03008		15	0,06359
34	0,06305		40	0,06393
35	0,03196		37	0,06715
36	0,03774		11	0,06919
37	0,06715		32	0,06968
38	0,04163		12	0,07233
39	0,05953		9	0,08518
40	0,06393		5	0,15342

Table 2: First step of C_i index calculation for the 4-layer MLPN

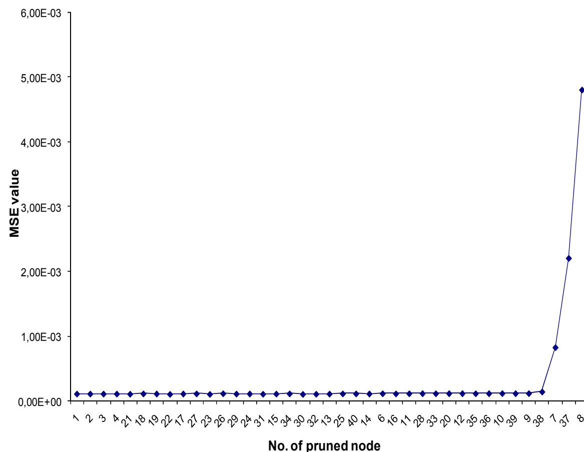

Fig. 10: MSE for the 4-layer MLPN during pruning

The final architectures of the MLPNs are shown in Figures 11 and 12.

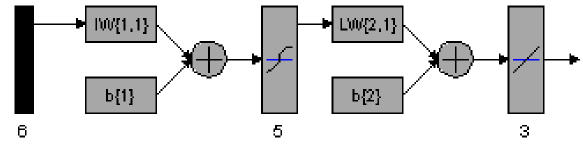

Fig. 11: Architecture of final 3-layer MLPN (6-5-3)

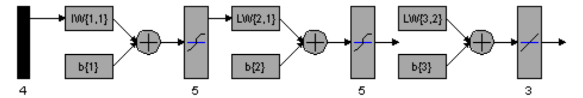

Fig. 12: Architecture of final 4-layer MLPN (4-5-5-3)

The prediction ability of these final architectures is tested using 5000 unseen IRs for which the target performances, namely the DC gain, *f_mech*, and *f_therm*, are known. This prediction ability is illustrated in the constellation plots of Figures 13–15. Each point corresponds to a MEMS instance. The blue and green points correspond to the 3-layer and 4-layer MLPN, respectively. The x-coordinate is the target (true) performance parameter value and the y-coordinate is the predicted performance parameter value. A very good correlation can be observed. This implies that we could substitute the expensive mechanical and thermal tests by processing the signature of pseudorandom test through trained MLPNs.

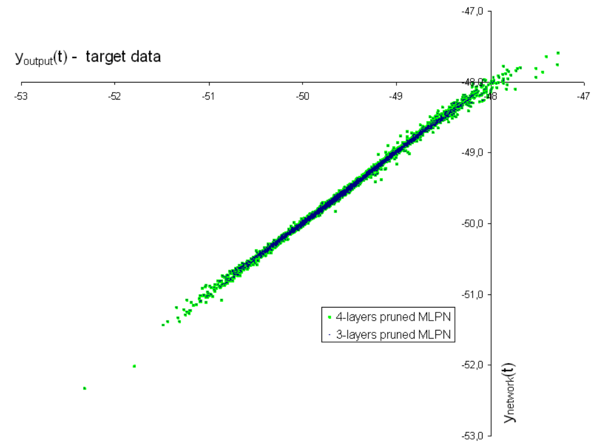

Fig. 13: Graph of approximation ability of final MLPNs – *DC gain*

5. DISCUSSION AND CONCLUSIONS

In this work, we propose a built-in test solution for MEMS devices that is based on mapping IR samples to the parameter specifications using MLPNs. This solution can significantly reduce the cost of MEMS testing by virtue of avoiding expensive thermal and mechanical tests. In comparison to [3], our method reduces the test error rate by

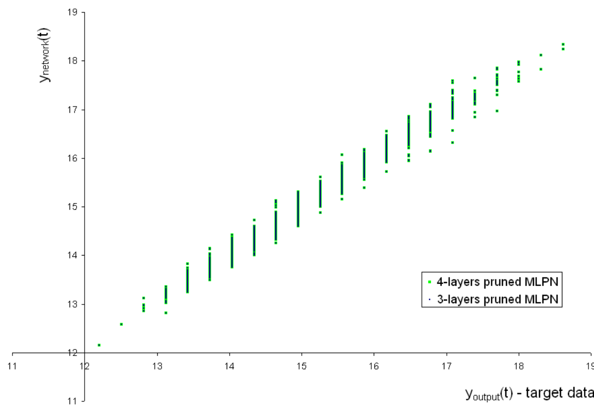

Fig. 14: Graph of approximation ability of final MLPNs – *f_therm*

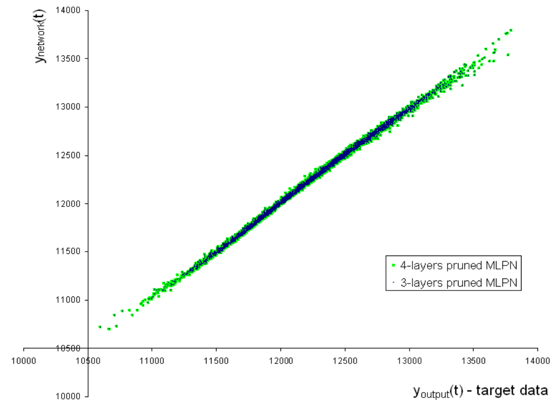

Fig. 15: Graph of approximation ability of final MLPNs – *f_mech*

avoiding crude comparison of IR samples to artificially imposed thresholds. Furthermore, the proposed method allows us to reduce the on-chip test circuitry which is peripheral to the MEMS device. This is achieved by a feature selection step which reduces the dimensionality of the IR signature and, therefore, the number of needed cross-correlation cells needed for extracting the IR signature. In terms of future work, we are planning to examine whether we can achieve similar prediction accuracy by using low-resolution IR samples that is by using converters with lower bit accuracy. This will further compact the needed built-in test resources.

ACKNOWLEDGMENTS

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